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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/066,095
	Filing Date	1/31/2002
	First Named Inventor	Steven Teig, et al.
	Group Art Unit	2825
	Examiner Name	Brandon Bowers
Total Number of Pages in This Submission	Attorney Docket Number	SPLX.P0074

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PATENT
Docket No. SPLX.P0074

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Mani Aden

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/066,095

Filing Date: 1/31/2002

For: METHOD AND APPARATUS FOR
IDENTIFYING A SET OF PATHS

Examiner: Brandon Bowers

Group Art Unit: 2825

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This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to

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Dated: August 24, 2004

Respectfully submitted,

By: _____

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/066,095
				Filing Date	1/31/2002
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	Brandon Bowers
Sheet	1	of	1	Attorney Docket Number	SPLX.P0074

FOREIGN PATENT DOCUMENTS								
Examiner* Initials	Cite No. ¹	Foreign Patent Document			Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code (if known) ⁵				
	1.	JP	02-262354		10-25-1990	Kuribayashi, Mototaka		

NON PATENT LITERATURE DOCUMENTS			
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	2.	CHO J.D., Wiring Space and Length Estimation in Two-Dimensional Arrays, May 2000, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, VOL. 19, Iss. 5, pp. 612-615.	
	3.	CONG J. et al., DUNE – A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.	
	4.	DION J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95-3, pp. 1-22.	
	5.	JUTTNER et al., "Lagrange Relaxation Based Method for the QoS Routing Problem, IEEE, Apr. 26, 2001, pp 259-268.	
	6.	SCHULZ U., Hierarchical Physical Design System, CompEuro '89, VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks. Proceedings, 8-12 May 1989, pp. 5/20 - 5/24.	
	7.	TSENG H-P. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.	

Examiner Signature		Date Considered	
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